IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s):   Young-Sik KIM, et al.

Serial No.:   09/773,874   Examiner: Mason, Donna K.

Filing Date: January 31, 2001   Group Art Unit: 2111

Confirmation No.:   7968

Title: SYSTEM ON A CHIP HAVING SYSTEM BUS, EXTERNAL BUS, AND
                    BUS ARBITER WITH PROGRAMMABLE PRIORITIES FOR BOTH
                    BUSES, SOFTWARE, AND METHOD FOR ASSIGNING
                    PROGRAMMABLE PRIORITIES

Mail Stop Amendment
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P.O. Box 1450
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PATENT & TRADEMARK OFFICE

INFORMATION DISCLOSURE STATEMENT

Sir:

This Information Disclosure Statement is submitted:

☒   under 37 CFR 1.97 (b); or
         (Within three months of filing national application; or date of entry of International
         application; or before mailing date of first office action on the merits; or before the
         mailing of a first Office Action after the filing of a request for continued examination
         under §1.114; whichever occurs last)

☒   Applicant(s) submit herewith Form PTO 1449-Information Disclosure Citation together
with copies of patents, publications or other information of which applicant(s) are aware, which
applicant(s) believe(s) may be material to the examination of this application and for which there may
be a duty to disclose in accordance with 37 CFR 1.56.

It is requested that the information disclosed herein be made of record in this application.

Any deficiency or overpayment should be charged or credited to deposit account number 13-
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Respectfully submitted,
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Atty. Docket No.:	9898-172
Applicant:	Young-Sik KIM, et al.
Filing Date:	January 31, 2001

Serial No.:	09/773,874
Group:	2111

INFORMATION DISCLOSURE CITATION
FORM PTO-1449 (Modified)

U.S. PATENT DOCUMENTS

Exam Init	Ref	Document Number	Issue Date	Name	Class	Sub Class
_____	_____	5,528,767	Jun. 18, '96	Chen		
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_____	_____	EP0518504	Dec. 16, '92	Europe	Fuoco, et al.
_____	_____	EP0564116	Oct. 6, '93	Europe	Drerup, et al.
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_____	_____	FR2674361	Sep. 25, '92	France	Chasserieau, et al.
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_____	_____	WO97/06523	Feb. 20, '97	PCT	G.R. Mohan Rao
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_____	_____	Bursky, D., "486 CPU Packs Peripherals for Real-Time System Needs," Electronic Design, vol. 43, no. 18, 5 Sep. 1995, pp. 167-168
_____	_____	Wingard, D., et al., "Integration Architecture for System-On-A-Chip Design," Custom Integrated Circuits Conference, IEEE, 11 May 1998, pp. 85-88

Examiner: _____

Date Considered: _____